Variable Gate Current Range Digital Gate Driver IC Always Providing 6-bit Controllability in Various IGBTs

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***Abstract*— To eliminate the need to redesign digital gate driver (DGD) ICs for each of a wide variety of power devices, the world's first variable gate current (I_G) range DGD (VIR-DGD) ICs with variable maximum I_G and resolutions are proposed. The innovation of VIR-DGD ICs is that a variable resistor on PCB allows one-bit I_G (I_{1BIT}) to be freely varied, thereby maintaining 6-bit controllability of DGD at all times for a wide variety of power devices. A 6-bit VIR-DGD IC with variable maximum I_G from 0.51 A to 5.1 A and I_{1BIT} from 8.1 mA to 81 mA has been developed. The trade-off problem between loss and noise during turn-on has been successfully solved by an active gate driving using the VIR-DGD IC for two types of IGBTs with twice the rated current.**

Keywords*— IGBT, IC, surge current, energy loss, active gate driver

I. Introduction

Digital gate drivers (DGD) ICs, which digitally change the gate current (I_G) multiple times in fine time slots during the switching period of power devices, are attracting attention as a technology that can solve the trade-off problem between loss and noise during power device switching [1-8]. In all conventional DGD ICs [1-8], the I_G range and steps are fixed for each IC. Different power devices require different I_G ranges and steps, which means that DGD ICs must be redesigned for each power device, which has been one of the challenges for the practical application of DGD ICs. For example, in a 6-bit DGD IC, when more than half of the maximum I_G is not needed, one bit of MSB is not used, and the IC operates as a 5-bit DGD, thereby preventing DGD from fully utilizing the original 6-bit I_G controllability. To solve the problem, in this paper, a world's first variable I_G range DGD (VIR-DGD) IC is proposed.

II. Proposed Variable I_G Range Digital Gate Driver IC

Figs. 1 and 2 show a circuit schematic and a timing chart of the proposed VIR-DGD IC, respectively. In the following, turn-on is discussed for simplicity, whereas the exact same is true for turn-off. This 6-bit DGD IC is based on the DGD IC in [6], and differs from [6] in the following two points: (1) the ability to change $V_{GS\,(PMOS)}$ amplitude of the 6-bit pMOSFETs in the output stage with an analog voltage ($CONT_{PMOS}$) via a variable resistor (R_2) on PCB to realize a variable I_G function, and (2) the addition of t_{ON}, t_{OFF} generator (TGEN), which generates the timing signals that define the time slots (t_{ON}) of the DGD using on-chip voltage controlled oscillators. The equation for I_G is shown in Fig. 1. The innovation of the VIR-DGD IC is that it can always achieve 6-bit controllability for a wide variety of power devices, because the 1-bit I_G (I_{1BIT}) is variable. As shown in Fig. 2, I_G can be varied 9 times with 6 bits (= 64 levels) in a t_{ON} time slot. Fig. 3 shows a die photo of VIR-DGD IC fabricated with 180-nm BCD process.

III. Measured Results

Fig. 4 shows the measured n_{PMOS} dependence of I_G at three different I_{1BIT} values of 81 mA (maximum value), 41 mA, and 0.51 mA (minimum value), where n_{PMOS} is a 6-bit control bit of I_G and is an integer from 0 to 63. To measure I_G, a 10 μF capacitor is connected to the output of DGD. As shown in Fig. 1, R_1 on PCB is fixed at 27 kΩ, and by varying the variable resistor R_2 on PCB, $V_{GS(PMOS)}$ amplitude is varied to change I_{1BIT}. Specifically, $V_{GS(PMOS)}$ amplitudes are 5.0 V, 3.0 V, and 1.7 V when I_{1BIT} is 81 mA, 41 mA, and 0.51 mA, respectively.Variable I_G range and I_{1BIT} are demonstrated.

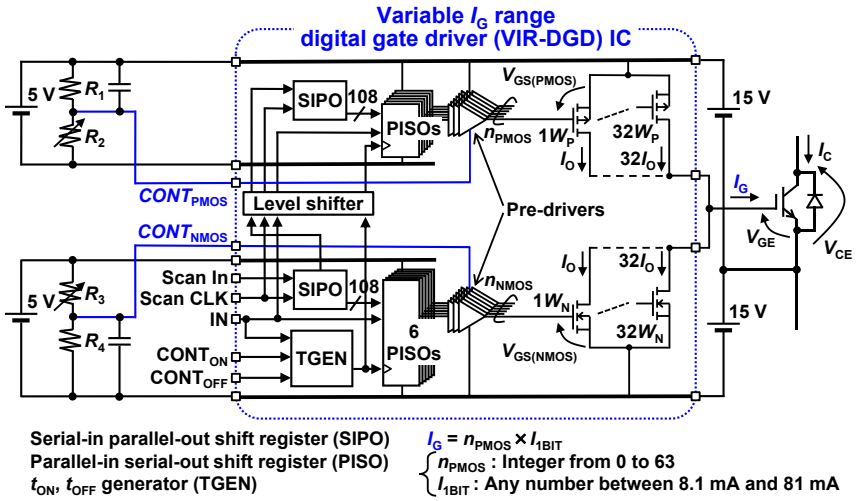


Fig. 1. Circuit schematic of proposed variable I_G range DGD (VIR-DGD) IC.

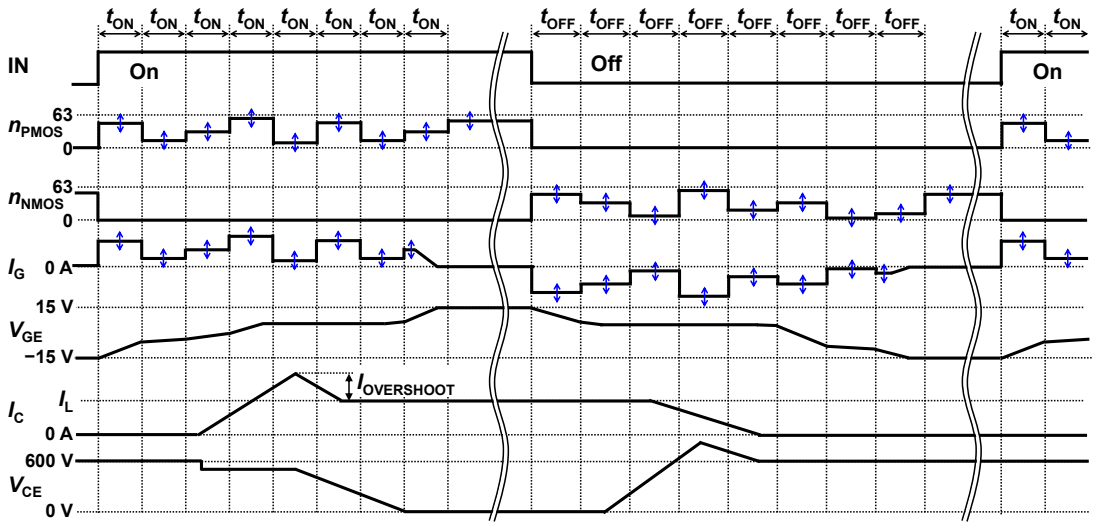


Fig. 2. Timing chart of proposed VIR-DGD IC.

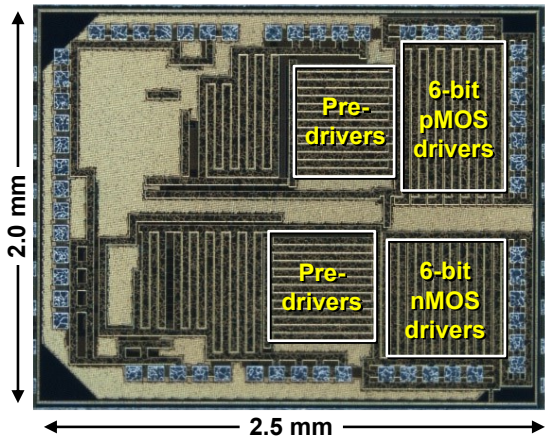


Fig. 3. Die photo of VIR-DGD IC.

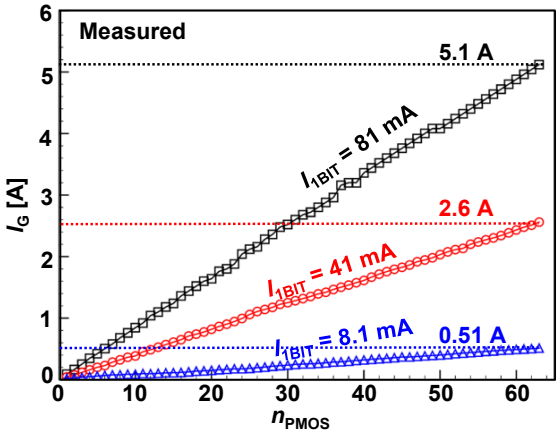
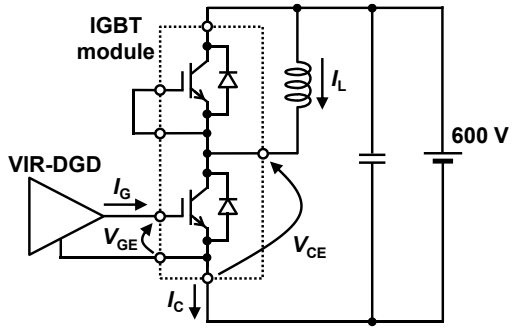


Fig. 4. Measured n_{PMOS} dependence of I_G at three I_{1BIT} values.

Figs. 5 and 6 show a circuit schematic and a measurement setup of the double pulse test using the developed VIR-DGD IC and IGBT modules, respectively. To demonstrate the functionality of the VIR-DGD IC, VIR-DGD IC with varied I_{1BIT} is applied to two types of IGBTs (IGBT1 and IGBT2)



Name	Model number	Rating	I_L	I_{1BIT}
IGBT1	FS100R12N2T4P	1200 V, 100 A	40 A	81 mA
IGBT2	FS50R12KT4_B11	1200 V, 50 A	20 A	41 mA

Fig. 5. Circuit schematic of double pulse test.

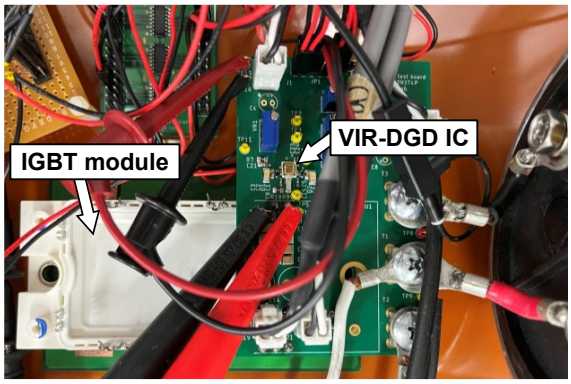


Fig. 6. Measurement setup.

with twice different current ratings, as shown in the table in Fig. 5. Figs. 7 (a) and (b) show timing charts of the conventional single-step gate driving (SGD) and the proposed active gate driving (AGD) at turn-on for comparison, respectively. In SGD, n is varied, which emulates a conventional gate driver with varied gate resistance. In AGD with 140 ns × 4 slots and last long slot, four parameters (n_1 to n_4) are varied.

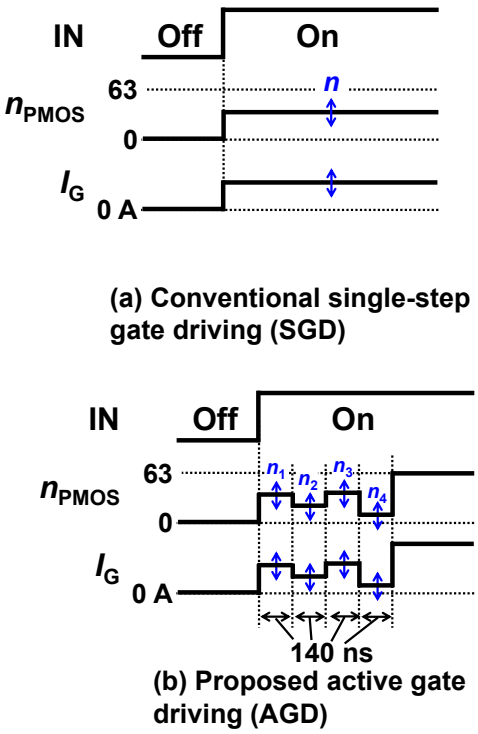


Fig. 7. Timing charts at turn-on. (a) Conventional single-step gate driving (SGD). (b) Proposed active gate driving (AGD).

Figs. 8 (a) and (b) show the measured switching loss (E_{LOSS}) vs. collector current overshoot ($I_{OVERSHOOT}$) of the conventional SGD and the proposed AGD in IGBT1 (load current (I_L) = 40 A, I_{1BIT} = 81 mA) and IGBT2 (I_L = 20 A, I_{1BIT} = 41 mA), respectively. The black curves show the trade-off curves for SGD with varying n. In this paper, an evaluation function (f_{OBJ}) shown in Eq. (1) [1-2, 8] is defined as a performance index of gate driving, and it is discussed that a gate driving with small f_{OBJ} is an excellent gate driving with small E_{LOSS} and $I_{OVERSHOOT}$.

$$f_{OBJ} = \sqrt{\left(\frac{E_{LOSS}}{E_{LOSS,\,MAX}}\right)^2 + \left(\frac{I_{OVERSHOOT}}{I_{OVERSHOOT,\,MAX}}\right)^2}, \qquad (1)$$

where the subscript MAX signifies the maximum of the corresponding quantity. The dotted concentric curves in Fig. 8 show the contour of f_{OBJ}. In the the proposed AGD, the double pulse tests are repeated more than 2500 times, and each time E_{LOSS} and $I_{OVERSHOOT}$ are measured to calculate f_{OBJ} defined in Eq. (1), and the combination of the four parameters (n_1 to n_4) that minimizes f_{OBJ} is searched using the simulated annealing algorithm [1].

In Fig. 8 (a), Points C and D are the best points with the smallest f_{OBJ} obtained by repeating the search for two trials. Since the simulated annealing algorithm cannot find the true optimal point, the optimal point obtained by the simulated annealing algorithm is different each time. Since Points C and D are nearly identical in Fig. 8 (a), this confirms that the search for the combination of the four parameters (n_1 to n_4) using the simulated annealing algorithm is reasonable. Points A and B are the conventional SGD points with $I_{OVERSHOOT}$ and E_{LOSS} approximately the same as the proposed Point C, respectively.

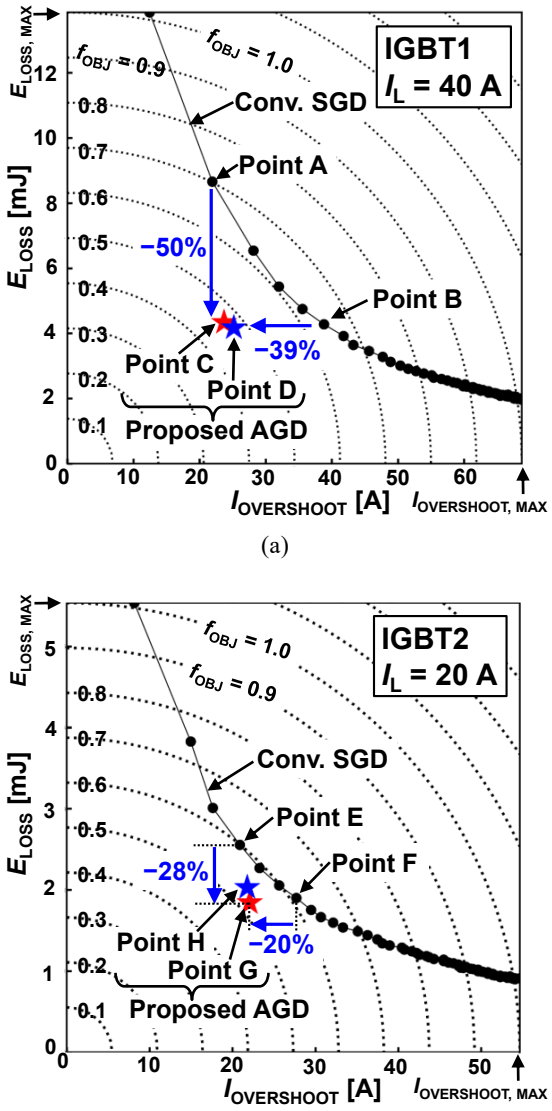


Fig. 8. Measured E_{LOSS} vs. $I_{OVERSHOOT}$. (a) IGBT1 (I_L = 40 A, I_{1BIT} = 81 mA). (b) IGBT2 (I_L = 20 A, I_{1BIT} = 41 mA).

As shown in Fig. 8 (a), compared with SGD, the proposed AGD (Point C) reduces E_{LOSS} by 50 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 39 % nder E_{LOSS}-aligned condition.

Fig. 8 (b) for IGBT2 (I_L = 20 A, I_{1BIT} = 41 mA) is exactly the same as Fig. 8 (a) for IGBT1 (I_L = 40 A, I_{1BIT} = 81 mA). Points G and H are the best points with the smallest f_{OBJ} obtained by repeating the search for two trials. Points E and F are the conventional SGD points with $I_{OVERSHOOT}$ and E_{LOSS} approximately the same as the proposed Point G, respectively. As shown in Fig. 8 (b), compared with SGD, the proposed AGD (Point G) reduces E_{LOSS} by 28 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 20 % nder E_{LOSS}-aligned condition.

Figs. 9 and 10 show corresponding measured waveforms of Points A to D in Fig. 8 (a) and Points E to H in Fig. 8 (b), respectively. In Fig. 9 (c), the proposed AGD (Point C) achieves low E_{LOSS} and $I_{OVERSHOOT}$ by setting n_{PMOS} to 1 just

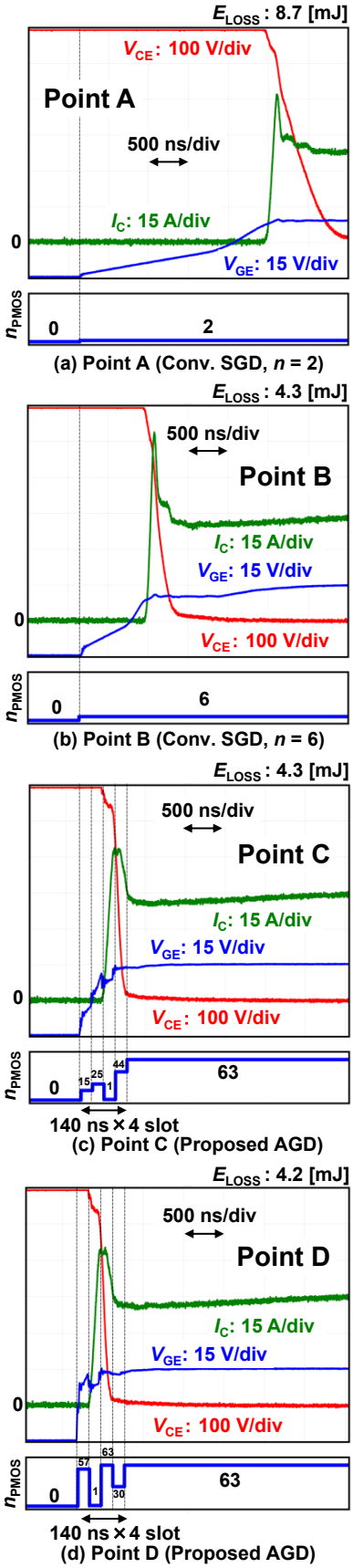


Fig. 9. Measured waveforms of Points A to D in Fig. 8 (a).

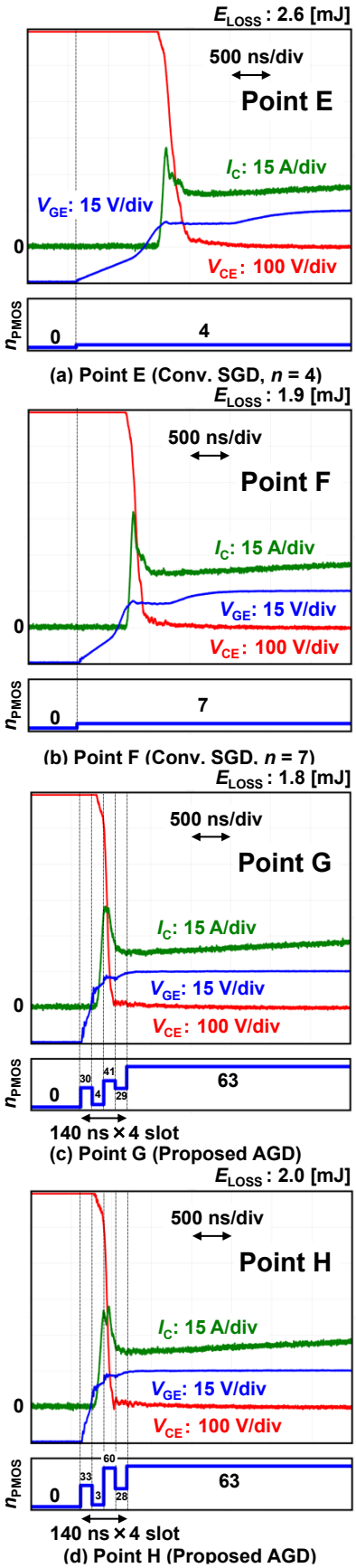


Fig. 10. Measured waveforms of Points E to H in Fig. 8 (b).

before the timing of $I_{OVERSHOOT}$. As shown in Figs. 9 (c) and (d), the optimal n_1 to n_4 for Points C and D obtained in the two trials are different, while E_{LOSS} and $I_{OVERSHOOT}$ of Points C and D are almost identical as shown in Fig. 8 (a). Similarly, as shown in Figs. 10 (c) and (d), the optimal n_1 to n_4 for Points G and H obtained in the two trials are different, while E_{LOSS} and $I_{OVERSHOOT}$ of Points G and H are almost identical as shown in Fig. 8 (b).

In this paper, the measured results of turn-off are not discussed, because the trade-off curves as shown in Figs. 8 (a) and (b) for E_{LOSS} and V_{CE} overshoot at turn-off were not observed. Table I shows a comparison table of DGD ICs. This work is the first to realize 6-bit DGD ICs with variable maximum I_G from 0.51 A to 5.1 A and I_{1BIT} from 8.1 mA to 81 mA, while achieving the 30 V output voltage swing required to drive IGBTs.

TABLE I. COMPARISON TABLE OF DGD ICS

	TPEL'21 [4]	TPEL'21 [3]	ECCE'22 [5]	TPEL'23 [7]	This work
Target power device	GaN FET	GaN FET	SiC MOSFET	SiC MOSFET	Si IGBT
Process	180 nm BCD	180 nm HV CMOS	180 nm BCD	500 nm HV CMOS	180 nm BCD
Max output voltage swing	4.8 V	5 V	30 V	18 V	30 V
I_G change per switching	8	104	3	30	9
Levels of I_G	7 bit	8 bit (coarse), 6 bit (fine)	6 bit	3 bit	6 bit
I_G range	Fixed	Fixed	Fixed	Fixed	Variable
Max I_G	4.8 V / 1.1 Ω = 4.4 A	5 V / 0.12 Ω = 42 A	22 A	3.6 A	0.51–5.1 A
1 bit of I_G (I_{1BIT})	35 mA	2.6 mA	340 mA	510 mA	8.1-81 mA

IV. CONCLUSIONS

The VIR-DGD ICs, which can always achieve 6-bit DGD controllability for a wide variety of power devices, are proposed to provide active gate driving with appropriate I_G steps at all times. To demonstrate the functionality of the VIR-DGD IC, VIR-DGD IC with varied I_{1BIT} is applied to two types of IGBTs icluding IGBT1 (100 A rating, I_L = 40 A, I_{1BIT} = 81 mA) and IGBT2 (50 A rating, I_L = 20 A, I_{1BIT} = 41 mA). In the turn-on measurements of IGBT1 and IGBT2 at 600 V, compared with the conventional SGD, the proposed AGD using VIR-DGD IC reduces E_{LOSS} by 50 % and 28 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 39 % and 20 % under E_{LOSS}-aligned condition, respectively.

ACKNOWLEDGMENT

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